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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/734,225	12/15/2003	Ha Ryong Yoon	40296-0047	8668

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EXAMINER

PATEL, ANAND B

ART UNIT PAPER NUMBER

2116

DATE MAILED: 11/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/734,225	Applicant(s) YOON, HA RYONG	
	Examiner Anand Patel	Art Unit 2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 September 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-8 and 10 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-8 and 10 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Amendment filed 9/22/06 has been entered and as such claim 1 is amended and claim 9 is canceled.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-2, 5-8, 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No 6496445 to Lee in view of US Patent No 5671258 to Burns et al (Burns).

- As per claim 1, Lee discloses a subsystem comprising:
 - A master (410) comprising a clock generator (column 6, lines 50-55) for generating a first clock signal (CLK1) and a second clock signal (CLK2) which have different frequencies from each other (column 5, line 63 – column 6, line 12; column 6, lines 55-61); and
 - A plurality of slaves (401-408) for receiving command and address signals from the master and transmitting data signals to the master (figure 4),
 - Wherein the first clock signal is used for the command and address signals (column 7, lines 1-7, 18-35), and the second clock signal is used for the data signals (column 7, lines 7-9, 18-35).
- Lee fails to disclose drivers for driving the clock signals. Burns teaches multiple clock drivers, each driving a clock signal (column 2, lines 47-52). Burns also teaches wherein the clock signals are in a predetermined ratio (column 2, lines 41-47). An advantage of the system taught by Burns is the ability to recover a clock signal without extra circuitry and wiring (column 2, lines 15-24). It would have been obvious to one of ordinary skill in the art at the time of invention to modify

Lee with the clock drivers as taught by Burns. Motivation to modify is to increase system reliability without increasing hardware costs.

- As per claim 2, Lee discloses the subsystem wherein the master transmits command and address signals into the corresponding slave only at a rising edge of the first clock signal (column 7, lines 24-27).
- As per claim 5, Lee discloses the subsystem wherein the slave is a memory module (401-408).
- As per claim 6, Lee discloses the subsystem wherein the frequency of the first clock signal is lower than that of the second clock signal (column 5, line 65 – column 6, line 1).
- As per claim 7, Lee discloses the subsystem wherein the clock generator is a clock synchronization means (920).
- As per claim 8, Lee discloses the subsystem wherein the clock generator further comprises a divider for dividing the first clock signal to generate the second clock signal (inherent given column 5, line 63 – column 6, line 12).
- As per claim 10, Lee discloses the subsystem wherein the clock synchronization means is a phase locked loop circuit (920).

4. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Burns and US Patent No 5345562 to Chen.

- As per claim 3, Lee and Burns fail to disclose the subsystem wherein the master transmits command and address signals into the corresponding slave only at a falling edge of the first clock signal. Chen teaches wherein the command and address signals are transmitted only at a falling edge of the clock signal (column 6, lines 17-22). An advantage of the system taught by Chen is the ability to ensure that equal access is given to write and read operations (column 4, lines 25-28). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Lee and Burns

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with the command and address transmission scheme as taught by Chen. Motivation to modify is to increase system efficiency by ensuring proper scheduling.

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee and Burns in view of US Patent No 5963502 to Watanabe et al (Watanabe).

- As per claim 4, Lee and Burns fail to disclose the subsystem wherein the master transmits command and address signals into the corresponding slave at the rising and falling edges of the first clock signal. Watanabe teaches wherein the command and address signals are transmitted at the rising and falling edges of the clock signal (column 1, lines 58-63). An advantage of the system taught by Watanabe is the ability to ensure proper timing of the memory system with regards to operating conditions (column 9, line 66 – column 10, line 13). It would have been obvious to one of ordinary skill in the art at the time of invention to modify Lee and Burns with the command and address transmission scheme as taught by Watanabe. Motivation to modify is to increase system reliability by ensuring proper timing.

Response to Arguments

6. Applicant's arguments filed 9/22/06 have been fully considered but they are not persuasive.
7. Applicant argues that Lee, Chen, and Watanabe do not disclose multiple clock drivers for producing clock signals. Examiner agrees. Burns is used to teach this limitation.
8. Applicant argues that Burns does not disclose the claimed clock generator. Examiner agrees. Lee discloses the majority of the claimed subject matter as indicated above. The limitation involving clock dividers to produce clock signals is taught by Burns. With the proper motivation cited above, one of ordinary skill in the art at the time of invention would have realized that the clock drivers taught by Burns could be used to create the clock signals within the system taught by Lee.

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9. Applicant further argues that Burns does not disclose that the frequencies of the clock signals are in a predetermined ratio. Examiner disagrees. Burns teaches two clock signals that are always a quarter cycle out of phase from each other. This implies that the frequencies will always be equal. Thus the ratio is predetermined to be one and the claim limitation is met.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

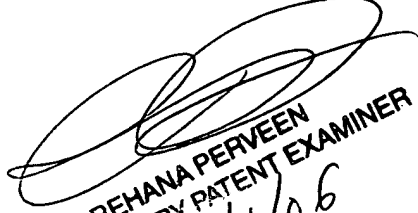
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anand Patel whose telephone number is (571) 272-7211. The examiner can normally be reached on Mon-Fri 8AM-4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on (571) 272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ABP



REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
11/1/06